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Vol. 1

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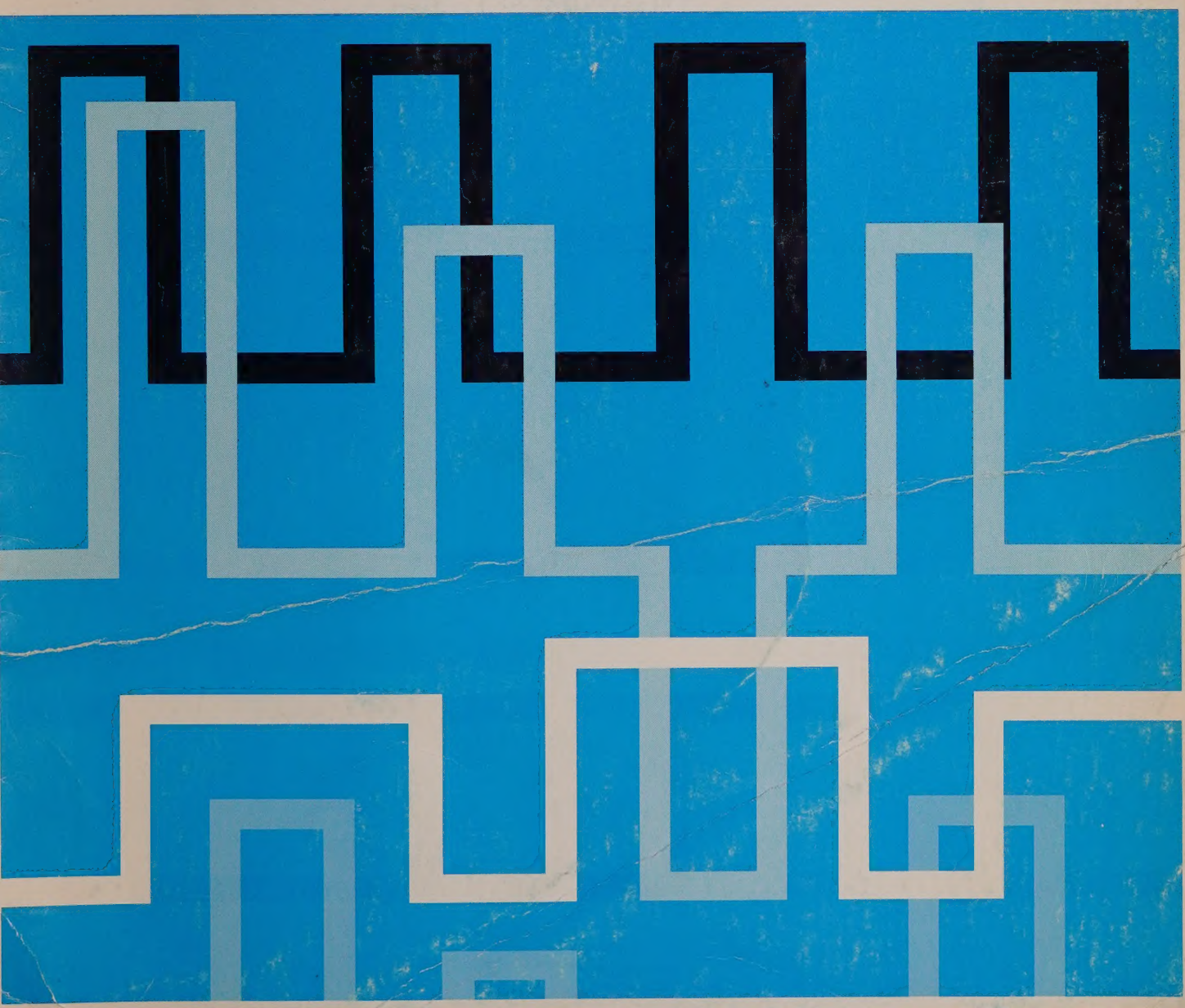

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INSTRUCTION MANUAL

MB-1A

BERT RECEIVER

ME7166

VOL 1 of 5

ME 7165

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INTRODUCTION

Using the Tau-Tron Model MB-1A PCM BERT Receiver, bit error rate measurements may be made on either pseudorandom or fixed data patterns. This important feature allows the use of non-pseudo-random, worst case patterns when exercising communications systems, magnetic tape/disk storage systems, or any other application where bit error rate measurements are made.

When analyzing pseudorandom patterns, the MB-1A can synchronize its internal code generator to any of six sequence lengths, and automatically recapture synchronization if sync loss should occur. For fixed data patterns, the user must supply an externally synchronized reference pattern along with the data under test. This allows the use of any non-pseudorandom data pattern desired to suit each individual application.

Four types of error measurement are displayed on the BCD LED readout: bit error rate (errors per time period), block error rate, errors per number of frames (each complete pseudorandom sequence, or fixed pattern word, is defined as one frame), or cumulative errors (totalize). Bit error rates as low as 1×10^{-10} can be displayed.

Various system warning and status indicators facilitate convient and reliable error measurements. Input clock/data skew can be adjusted via front panel control.

SPECIFICATIONS

All front panel input/output signals are standard TMI levels as defined at the end of this section.

INPUTS

CLOCK IN---From 1 Hz to 75 MHz. 5 ns minimum width.

DATA IN---NRZ format. Data upon which error rate measurements are to be taken.

EXT CMMND IN---External Command input; initiates error detection resynchronization. Minimum pulse width = 50 ns.

CLEAR IN---Parallels function of pushbutton; clears internal counters and display, resets synchronization logic to "in sync" status.

GATE IN---Gates the error detector and time base counters. Freezes the current error measurement status. High level inhibits, low level enables.

FX DATA IN---Reference data pattern for fixed pattern error rate measurements.

FX SYNC IN---Reference sync pulse signal for defining fixed pattern frames in Frame Rate measurements. Also necessary to provide SYNC OUT in FX mode.

OUTPUTS

CLOCK OUT---Fixed width pulse at CLOCK IN frequency; typically 5 ns width.

SYNC OUT---One clock period wide pulse, occurring once every 2^N-1 bit PN frame or follows FX SYNC IN, depending on reference data mode selected.

ERROR OUT---Error comparator output. Fixed width pulse, typically 5 ns.

TIME BASE OUT---Output of time base counter.

OUT OF SYNC---Burst error indication. True during burst error condition. False when in sync.

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CONTROLS

Clock/Data PHASE---Adjustment delays clock input with respect to data inputs over range 0 to 30 ns, or 50% duty cycle minus 5 nsec, whichever is less.

PN/FX---Selects reference data as either internal PN code generator, or external (FX) input.

CODE LENGTH Selection---Choice of six PN code lengths generated by internal PN generator. All codes are maximum length PRBS. Length = 2^N-1; where N = 6, 9, 11, 15, 17, or 20.

AUTO/EXT COMMND/MANUAL---Selects synchronization mode. AUTO will automatically search for synchronization when the average error rate exceeds a fixed error threshold. EXT COMMND will attempt synchronization whenever commanded by an external input. MANUAL will attempt synchronization whenever commanded by the associated pushbutton.

LOW/HIGH THRESHOLD---Choice of two threshold levels, both represent a 20% average error rate. LOW selects 20 errors in 100 bits. HIGH selects 500 errors in 2500 bits.

BIT/BLOCK RATE---Displayed ERROR COUNT may represent either bits or blocks in error as selected by this control. BIT RATE is 1 error counted per bit error. BLOCK RATE is 1 error counted per erroneous block: one or more bit errors within 10, 100, or 1000 bit block.

TIME RATE/FRAME/TOTALIZE---Three modes of error measurement are possible. FRAME RATE computes errors per multiple of frame sync selected by the TIME BASE x 10^N thumbwheel. TIME RATE computes errors per multiple of clock periods selected by the TIME BASE x 10^N thumbwheel. TOTALIZE simply accumulates errors indefinitely.

CLEAR---Clears internal counters and displays, resets synchronization logic to "in sync" status.

TIME BASE x 10^N---Time base for frame rate and time rate is frame sync and clock respectively, multipled by 10^N; where N = 0 through 10.

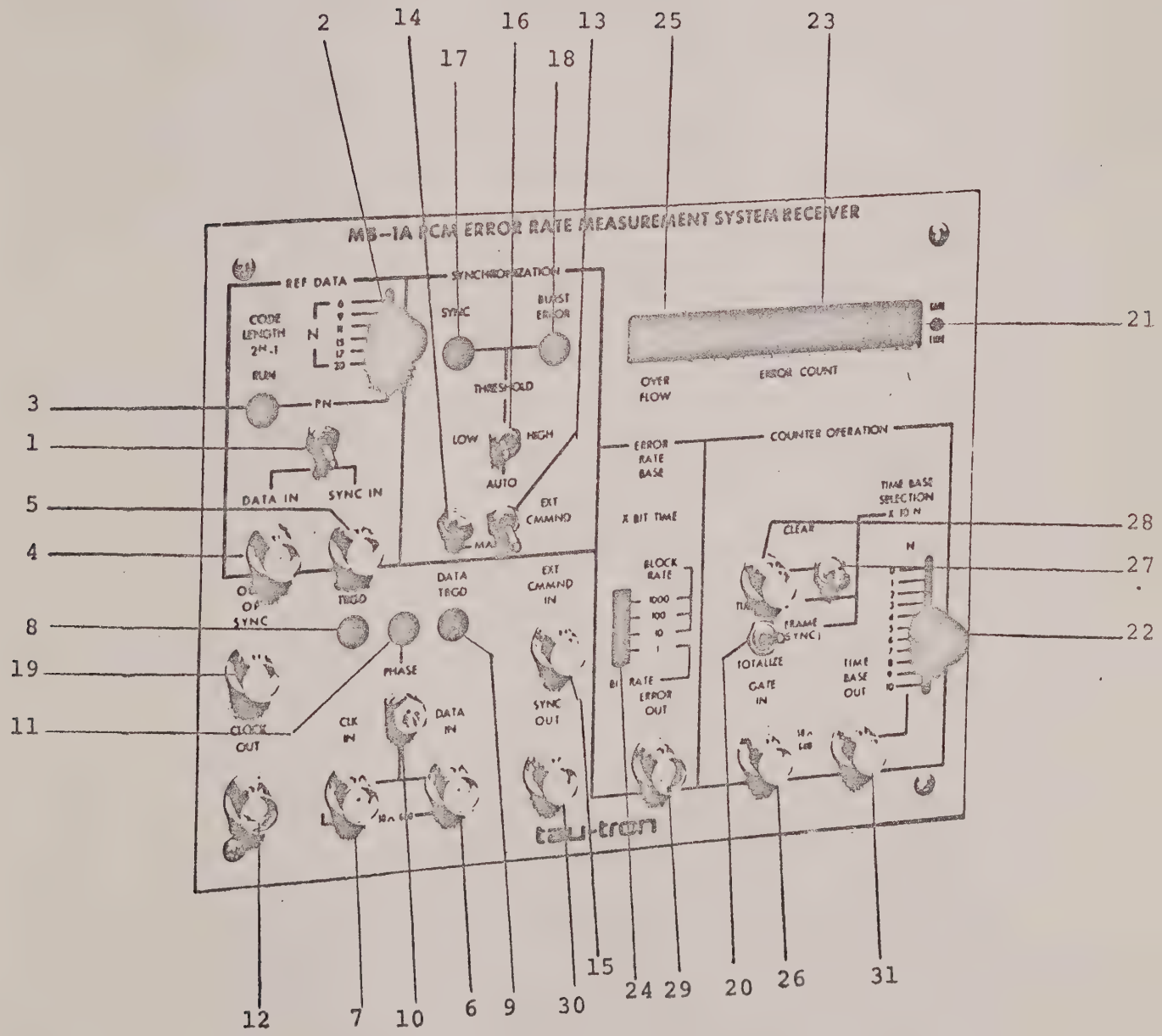
DISPLAYS AND INDICATORS

CLOCK TRGD---Indicates acceptable input clock levels (clock triggered).
DATA TRGD---Indicates acceptable data input levels (data triggered).
PHASE---Indicates proper clock/data phase relationship.
RUN---Indicates PN code generator is operating.
SYNC---Indicates that reference code and input data are "in sync"; error rate less than selected threshold.
BURST ERROR---Indicates that a burst error has occurred; error rate has exceeded the selected threshold.
GATE TIME---Indicates that error measurement is taking place. Always "on" in TOTALIZE.
ERROR COUNT AND OVERFLOW---Display value of selected measurement up to 9999 with overflow indicator. Display option provides one or two additional digits (up to 999999), if desired.

PRINTER INTERFACE---Rear panel. All signals TTL compatible.
DISPLAY CONTENTS---All digits (BCD) plus overflow.
CLEAR---Clears internal counters and displays. Does not affect synchronization logic.
ENABLE (DATA LOGGING)---Freezes contents of display.
PRINT STROBE---Drives an external printer.
BUSY---Accepts busy signal from an external printer; freezes contents of display and inhibits print strobe.
INTERROGATE---Forces a print strobe to occur.
PRINTER OFF---Must be driven low, or grounded, to indicate that a Printer is connected; and to enable printer interface logic.

STANDARD TMI SIGNALS

Logical Zero---Between -200 and +600 mv.
Logical One---More positive than 1.7 volts.
Standard Amplitude---2.0 volts typical.
Transition Edges---Typically 2 ns, 3.5 ns maximum.
Impedance---50 ohms to system ground.
Waveshape Distortion---Less than ±7%, terminated properly.


MB-1A PCM ERROR RATE MEASUREMENT SYSTEM RECEIVER
REF DATA
SYNCHRONIZATION
CODE LENGTH 2^N-1
N
L
RUN
PN
SYNC
BURST ERROR
THRESHOLD
LOW
HIGH
AUTO
DATA IN
SYNC IN
EXT CMMND
OVER FLOW
ERROR COUNT
ERROR RATE BASE
COUNTER OPERATION
X BIT TIME
BLOCK RATE
1000
100
10
1
BIT RATE ERROR OUT
TIME BASE SELECTION X 10 N
CLEAR
TOTALIZE
FRAME (SYNC)
GATE IN
TIME BASE OUT
OUT OF SYNC
TRIGD
DATA TRGD
EXT CMMND IN
PHASE
CLOCK OUT
CLK IN
DATA IN
SYNC OUT
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OPERATING INSTRUCTIONS

NOTE: Numbers in parenthesis correspond to numbers on front panel illustration.

REFERENCE DATA

MB-1A can perform error rate measurement on any data pattern, including pseudorandom data patterns. An internal pseudorandom (PN) data generator can be utilized for PN error rate measurement by selecting PN (1) reference mode. A six position slide switch (2) is then used to select the PN code length. All PN codes generated internally are maximum length; i.e. they contain 2^N-1 bits, where N is the number of binary stages in the code generator.

N = 6	Code Length = 63 bits
N = 9	Code Length = 511 bits
N = 11	Code Length = 2047 bits
N = 15	Code Length = 32767 bits
N = 17	Code Length = 131071 bits
N = 20	Code Length = 1048575 bits

When the PN code generator is operating, the RUN indicator (3) will be "on".

For fixed (FX) data patterns, or any desired pattern from an external source, the FX reference mode (1) is selected. In this mode, the reference pattern must be supplied properly aligned to the data under test. The internal synchronization logic will not be able to perform synchronization of the reference code, and serves only as an in sync/out of sync detector. FX DATA IN (4) is the reference data input. If frame rate measurements are desired when using FX mode, a frame sync signal must be supplied to the FX SYNC IN (5). This signal need not be aligned to either data or clock inputs. FX DATA IN should be NRZ.

TEST DATA

Both the test data (6) and a properly aligned clock (7) must be supplied to the MB-1A. Test data should be NRZ format. Clock can be pulse or rectangular waveform. Minimum pulse width is 5 ns. Maximum frequency is 75 MHz.

CLOCK TRGD (8) (triggered) and DATA TRGD (9) (triggered) LED's indicate when proper input levels are present. A clock/data phase adjustment (10) and indicator (11) allow fine adjustments to be made with ease. Fully counter-clockwise is minimum clock delay. Care must be taken to insure that this adjustment is set no greater than 50% duty cycle minus 5 ns. Otherwise, the clock will divide-by-2 internally. In PN mode, this cannot be detected from observing the front panel displays. The best method is to observe the CLOCK output (12) on an oscilliscope and insure that it is at the same frequency as the input clock. Optimum clock/data phasing is achieved at clock leading data by 5 to 10 ns.

SYNCHRONIZATION

For PN testing, the internal code generator can be synchronized to the test data by three methods. In MANUAL (13) mode, the internal generator is synchronized each time the MANUAL (14) pushbutton is depressed. In EXT COMMND (13) mode, an external command input (15) is required to initiate PN code generator synchronization. A positive pulse should be used. In AUTO (13) mode, resynchronization will occur whenever the bit error rate exceeds 20%.

For FX testing, synchronization must be provided for externally by properly aligning the reference data input (4) to the test data (6) input. The two signals should be aligned bit-by-bit. AUTO (13) mode is disabled; the other two synchronization modes have no effect other than setting the sync status to "In Sync".

In sync/out of sync threshold is always a 20% bit error rate. However, two threshold selections are possible, depending on the error burst characteristics of the system under test. LOW THRESHOLD (16) is 20 errors out of 100 bits. This setting will detect an out of sync condition much faster, but is susceptible to error bursts: small periods of high error rate where the longer average is much lower than 20%. For this reason, HIGH THRESHOLD (16) is provided. In this position 500 errors out of 2500 bits is required for an out of sync condition. When an out of sync condition is detected, resynchronization is immediately initiated in AUTO (13) PN (1) mode.

Two indicators show whether the reference code is in SYNC (17) or out of sync (18) (BURST ERROR). Additionally, a front panel output (19) goes true whenever an out of sync condition is present.

COUNTER SECTION

Three counter modes are possible: Frame Rate, Time Rate and Totalize. These modes of operation will be described in the next three sections.

FRAME RATE

In this counter mode, the time base counter is driven from the frame (data) sync signal; either generated internally by the PN code generator, or supplied externally via the FX SYNC IN (5). The counter mode (20) switch is placed in the FRAME position.

Errors will now be counted for the duration of the GATE TIME (21), or error window. This error window is opened and closed by overflows of the selected time base counter output. Either the frame sync itself, or any decade multiple of the frame sync as selected by the TIME BASE x 10^N (22) side switch, will control the error window.

Either bit errors or block errors may be counted, as selected by the BIT RATE/BLOCK RATE (24) switch. In bit rate (equivalent to a block size of 1 bit), the ERROR COUNT (23) will read as bit errors per frame, bit errors per 10 frames, bit errors per 100 frames, etc. In any of three block rate positions, the ERROR COUNT (23) reads as block errors per frame, etc. Whether or not a block error measurement in FRAME mode has meaning depends on frame size (sequence length), block size (10, 100, 1000 bits), and the application. For example, a block size of 1000 bits with a time base of 1 63-bit frame, or 10 63-bit frames (630 bits) will not be too meaningful. Normally block size should be smaller than the time base size selected.

The maximum value of the error counter is 9999 errors (unless optional digits are installed). An OVERFLOW (25) indicator will turn on should the errors be in excess of the maximum value.

TIME RATE

In this counter mode, the time base counter is driven either by the input clock, or a decade multiple of the input clock, as selected by the BIT RATE/BLOCK RATE (24) switch. The error counter is driven either by bit errors or block errors, as determined by the same switch (24). To select this counter mode, the counter mode (20) switch is placed in the TIME RATE position.

When bit rate has been selected (24), the errors are counted as described earlier for FRAME mode. An error window is opened and closed by overflows from the time base counter. However, the 0 position of the TIME BASE x 10^N (22) slide switch is now meaningless (errors per bit). Bit error rate is read directly from the ERROR COUNT (23) display; i.e. bit errors per 10 bits, bit errors per 100 bits, etc.

When a block rate (10 bits, 100 bits, 1000 bits) has been selected (24),the errors that are counted are block errors. This is defined as 1 block error if one or more bit errors occur within a block. An error window is generated, as before, by overflows from the time base counter. However, the time base counter is now driven from the block prescaler, not the input clock. This means that the error window is controlled by the block prescaler, or any decade multiple of the block prescaler as selected by the TIME BASE x 10^N (22) slide switch. The 0 setting of this control is still meaningless (block error per block). Other block error rates are read directly from the ERROR COUNT (23) display; i.e. block errors per 10 blocks, block errors per 100 blocks, block errors per 1000 blocks, etc.

The maximum value of the error counter is 9999 errors (unless display options are installed). An OVERFLOW (25) indicator will turn on should the errors be in excess of the maximum value.

TOTALIZE

In this counter mode, the time base counter is disabled. The counter mode (20) switch is placed in the TOTALIZE position.

An infinite error window is created internally, and the GATE TIME (21) will be on continuously. Errors will be counted and displayed as they occur; always showing the total cumulative errors since the error counter was last reset. If desired, external error windows can be created by applying a high level to GATE IN (26) to freeze the internal counters. GATE IN (26) does not affect the GATE TIME (21) LED. A maximum of 9999 errors (unless display options installed) can be accumulated before OVERFLOW (25) occurs.

CLEAR FUNCTION

As described in the specifications section, pressing the CLEAR (27) pushbutton, or raising the CLEAR IN (28) signal to, a high level, causes initialization of the machine: all error counters are reset, the display contents are cleared, and the time base counter is preset (so that the error window can open promptly when the time base counter overflows). The synchronization logic is set to "in sync" status. A remote clear input on the printer interface causes essentially the same reaction, except that it has no effect on the synchronization logic. The clear function is level sensitive, and no operation is possible if any of the clear inputs (signal or manual) is true.

AUXILLIARY OUTPUTS

Several auxilliary outputs are provided both as a monitor of machine operation and to enhance the versatility of the machine.

An ERROR OUT (29) monitor provides a fixed 5 ns pulse for each error detected. This output is gated by the GATE IN (26) signal.

A SYNC OUT (30) provides a sync output pulse, one clock period wide, once per pseudorandom frame in PN (1) mode. In FX (1) mode it follows the FX SYNC IN (5) signal.

A TIME BASE OUT (31) monitor is provided. This follows the internal time base counter output as selected by the TIME BASE x 10^N (22) slide switch. Internally, this signal overflows to open and close the error window in frame and time rate modes.

A CLOCK OUT (12) is provided which is a fixed 5 ns pulse at the input clock rate. This monitor can be used to insure that the duty cycle of the PHASE (10) control has not been exceeded; since the frequency of this signal becomes input clock ÷2 when duty cycle is exceeded.

An OUT OF SYNC (19) monitor indicates "in sync" (low level) and "out of sync" (high level) status.

TIMING CONSIDERATIONS

As discussed in the operating procedure section on the phase adjust control, the ideal timing for the CLOCK IN (7)/DATA IN (6) signals is 5 ns clock leading data. An indicator is provided to show when these two signals are properly phased (11), and adjustment (10) of the phasing is easily made. Note: When using the MMX-1 DATA FORMATTER and MG-3B DATA GENERATOR, the phase adjust should remain fully counter clockwise at the maximum clock frequency. All other timing will be correct if the MMX-1 interconnection rules are followed.

The FX DATA IN (4) should be bit synchronous with the DATA IN (6) and edge aligned. Bit no. 1 of each data input must be aligned and keeping proper bit-by-bit alignment is an external responsibility. Internal synchronization logic can not realign these inputs if synchronization is lost.

Alignment of FX SYNC IN (5) is not necessary. This signal should be synchronous with the FX DATA IN (4) word frame.

EXT CMMND IN (15) can occur at any time desired by the user. No alignment is necessary other than that necessary for the user's test set-up.

GATE IN (26) can also occur at any time desired by the user. DATA IN (6) should represent valid data to be measured when the GATE IN (26) is low.

CLEAR IN (28) may also occur at any time. When using the GATE IN (26) input, the usual procedure is to issue CLEAR IN (28) while the gate signal is high (disabled).

PRINTER INTERFACE

The printer interface provides BCD outputs of the contents of the front panel display, including an overflow signal, along with suitable printer control signals. All outputs are TTL compatible and capable of driving up to 3 normal (7400) TTL loads. Print strobe and printer hold controls, of selectable polarity, make this output compatible with many common digital printers. Connector pin-out is given in Table 1.

All display digits plus the overflow signal are available. These outputs are positive true: a high level indicates logic one. The least significant bit of the least significant digit is $1\text{-}2^{0}$. The number before the dash is the decade. The number after the dash indicates BCD weight (8421 code).

Six control signals are present and are defined below:

1. $\overline{\text{CLEAR}}$---Accepts a negative true TTL input. When at a low level, clear function is asserted as described in an earlier section. Loading is one TTL (7400) load plus 1K resistor pullup to +5 volts. Minimum width is 50 ns.
2. ENABLE (DATA LOGGING)---Accepts a negative true TTL input. When at a low level, the display is frozen. This allows for synchronization of display read out, if necessary, with an external controller, such as a computer. Loading is one TTL (7400) load plus 1 K resistor pull up to +5 volts.
3. PRINT STROBE---Either a positive or negative true printer strobe pulse. This should cause the printer to print the display outputs described above; and also to advance one line. The width of the strobe pulse is determined by the RC components (R49, C1) of the 74123 on the INTERFACE and PRINTER PC card. Polarity is determined by a jumper on the same PC card at B3 pin 13. Unless specified otherwise at time of order, polarity is supplied positive and width is supplied at 10 ms.

4. BUSY---Accepts either a positive or negative true TTL input from the printer. This signal will freeze the contents of the display and inhibit further print strobes until the printer is ready for the next print cycle. After the trailing edge of BUSY the display will remain frozen and the print strobe inhibited for a period of time determined by the RC components (R60, C2) of the 74123 on the INTERFACE and PRINTER PC card. Polarity is determined by a jumper on the same PC card at B3 pin 9. Many common printers have a hold off requirement after their BUSY output ends. Unless specified otherwise at time of order, polarity is negative and hold off is 100 ms.
5. $\overline{\text{INTERROGATE}}$---Accepts a negative-going TTL strobe input. For TOTALIZE mode where no internal print strobe occurs; or for asynchronous print strobes, this input will initiate a print strobe/display freeze cycle at the negative transition of its input level. Loading is one TTL (7400) load plus 1K resistor pull up to +5 volts. Minimum width is 50 ns.
6. PRINTER OFF---Accepts a positive true TTL input. The printer control logic is only enabled when this input is a low level. May be grounded when a printer is connected; and left open when the printer is not connected. Loading is one TTL (7402) load plus 1K resistor pull up to +5 volts.

Mating connector is 50 pin Amphenol plug, Blue Ribbon Series, #57-30500.

TABLE 1

PRINTER INTERFACE CONNECTOR PIN OUT

PIN	SIGNAL		PIN	SIGNAL
1	$1\text{-}2^0$		26	$\overline{\text{CLEAR}}$
2	$1\text{-}2^1$		27	ENABLE (DATA LOGGIN
3	$1\text{-}2^2$		28	PRINT STROBE
4	$1\text{-}2^3$		29	BUSY
5	$10\text{-}2^0$		30	$\overline{\text{INTERROGATE}}$
6	$10\text{-}2^1$		31	PRINTER OFF
7	$10\text{-}2^2$		32	
8	$10\text{-}2^3$		33	
9	$100\text{-}2^0$		34	
10	$100\text{-}2^1$		35	
11	$100\text{-}2^2$		36	
12	$100\text{-}2^3$		37	NOT USED
13	$1000\text{-}2^0$	DISPLAY CONTENTS	38	
14	$1000\text{-}2^1$		39	
15	$1000\text{-}2^2$		40	
16	$1000\text{-}2^3$		41	
17	$10000\text{-}2^0$		42	
18	$10000\text{-}2^1$		43	
19	$10000\text{-}2^2$		44	
20	$10000\text{-}2^3$		45	
21	$100000\text{-}2^0$	OPTIONAL	46	GROUND
22	$100000\text{-}2^1$		47	
23	$100000\text{-}2^2$		48	
24	$100000\text{-}2^3$		49	
25	Overflow		50	

THEORY OF OPERATION

MB-1A, Error Rate Measurement Receiver, incorporates two major functions into a single unit: bit error detection and error rate measurement. Bit errors can be detected for fixed patterns as well as the more usual pseudorandom patterns. Error rate measurements can be the normal modes of frame error rate, time error rate, and total cumulative errors. In addition, block error rate measurements can be made.

A Block Diagram is included with the schematic in the manual.

ERROR DETECTION

Errors are detected on a bit-by-bit basis for two types of input data: pseudorandom or fixed patterns. The basic differences in operation are that an internal reference code generator is used for pseudorandom detection and the synchronization of the reference code to the incoming data can be controlled internally. This allows re-synchronization of the reference code generator if a burst error condition occurs.

With fixed pattern error detection, the reference code generator is external to the MB-1A, and all synchronization of the reference code to the incoming data must be done externally.

PN ERROR DETECTION

The internal reference code generator used in this mode of operation is located on the PR NUMBER GENERATOR card. A pseudorandom (PN) code can be generated by a shift register with appropriate feedback taps. While many combinations of feedback taps are possible, only the proper combinations of taps will produce a maximum length pseudorandom code; i.e. the code length equals (2^N-1) bits, where N is the number of shift register stages. Since the feedback signals are logically exclusive-or'ed at the shift register input, the all zeroes state of the shift register becomes an illegal state, accounting for the "-1" factor.

In the MB-1A, maximum codes are produced for shift registers which have 6, 9, 11, 15, 17, and 20 stages (selections 1 through 6 respectively in the lower left corner of the schematic). The taps for these code lengths are listed on the schematic. For reasons of propagation delay in high speed shift registers, the generator is implemented so that there is never more than two gate delays between register stages, even at the shift register input. This requires that a delta register be used to set up the number of stages between the last stage tap and the mid-stage tap. The mid-stage tap is one fixed input to the exclusive-or circuit, and the gate multiplexer sets up the appropriate number of stages to the fixed last stage flip-flop. Also the appropriate number of stages from the first stage to the mid-stage is set up by a second gate multiplexer. Using this high speed method restricts the lengths of maximum-length PN codes generated to those with only two taps within range of the delta register. Deltas for each PN code length are also shown on the schematic.

Since the all zeroes state is illegal, a zero detector is used to monitor the number of active stages for the code length selected. Should all zeroes be detected at power-on or any other time, the first stage would be forced to a logic one. To conserve on logic, the PN sync detector is implemented in the zero detector. A PN sync is generated whenever the shift register contains a logic one in its first stage, and a logic zero is all other stages.

Incoming data is received on this card and compared to the reference data output by a exclusive-or circuit. Whenever a bit-by-bit mismatch is detected, an NRZ error signal is sent to the INTERFACE and PRINTER card.

FX ERROR DETECTION

Since the reference generator is external to the MB-1A, the FX reference pattern is received on the INTERFACE and PRINTER card, along with an incoming data signal from the PR NUMBER GENERATOR card. Here both signals are compared on a bit-by-bit basis by an exclusive-or circuit. The NRZ output of this error detector is

multiplexed with the PN NRZ error signal. Depending on front panel control setting, one of these signals is converted to RZ error signals for use by the error measurement logic. RZ errors are gated with the gate signal received on this card before driving the RESYNC CONTROL card.

FX Sync is received from the external reference generator on the PR NUMBER GENERATOR CARD, where the control setting determines which SYNC signal (FX or PN) is sent to the TIME BASE COUNTER card.

SYNCHRONIZATION

For FX mode, synchronization is assumed at the front panel inputs. For PN mode, the synchronization is controlled by the RESYNC CONTROL card. In either mode, burst error conditions are detected on this card.

RZ errors and clock drive this card, which contains two types of counters. The clock drives a time base counter which determines whether 100 bits (clock periods) or 2500 bits have occurred. Overflows from this counter reset the error counter driven by the RZ errors. Should either 20 or 500 errors (depending on control setting) occur before the error counter is reset, the error counter overflow would set the out-of-sync latch. This causes the front panel sync status indicators to change state, and drives the OUT OF SYNC output true.

Depending on control settings; either a manual pushbutton signal, or an external resync command input may be required to cause resync. In automatic resync mode, whenever out-of-sync is detected, resync occurs.

By one of the means above, the resync control logic is triggered. Using overflows of the first decade of the time base counter on this card, a 20-bit resync control signal is generated which causes the PN reference generator to feed the incoming data directly into the first stage of the shift register (feed forward operation). After 20 bits have entered the PN generator shift register, feedback

operation is restored and the generator is assumed to be in sync with the incoming PN code (which is true if the 20 bits were error-free). At the same time, the out-of-sync status is reset to show in sync.

In FX mode, the auto resync mode is inhibited because the resulting in sync status would be meaningless since the resync control signal cannot affect the synchronization of the external reference generator.

CLOCK PHASING

The clock input is received on the PR NUMBER GENERATOR card, where the clock/data phase control and detector are located. Phasing is adjusted by controlling the amount of delay in the input clock path with reference to the input data path. The range of the control is at least 30 ns, so it is possible to have delay settings in excess of the input clock period.

Care must be taken when adjusting the delay control, since the delay circuit is capable of only about 50% duty cycle. Further, 5 ns circuit delays reduce the effective range to 5 ns less than 50% duty cycle (input clock period).

ERROR RATE MEASUREMENT

As previously mentioned both the normal measurements of frame rate, time rate, totalize; and block error measurements can be made with the MB-1A. The normal measurements are only concerned with how many errors occurred (as a rate or cumulative measurement). Block error measurements give insight into the manner in which errors occur.

NORMAL ERROR MEASUREMENTS

In all three modes: frame rate, time rate, and totalize, the RZ error signal from the RESYNC CONTROL card drives a decade ripple counter. The first decade is located on the COUNTER card. Succeeding decades are located on the DISPLAY card. From the third decade on, the BCD counter is internal to the LED display I.C.

The difference between totalize and either error rate mode is the amount of time during which errors are allowed to trigger the error counter. In totalize, this error window is infinite; i.e. open all the time. Errors are accumulated until a clear command is received.

In both of the error rate modes, overflow of the selected time base drives an error window circuit. Two overflows are required to first open, then close the error window. This error window permits triggering of the error counter and drives the GATE TIME indicator. Once closed, the process cannot repeat itself until the display hold times out, permitting visual read out of the error rate. After display hold time out, the error window generator and the error counter are both reset.

The error window generator and time base counter are located on the COUNTER card. A ten digit decade counter is used. In frame rate mode, this counter is driven by the data frame sync. In time rate mode, this counter is driven by the input clock (bit error rate). A gate multiplexer is used to select the desired time base: either the counter trigger signal itself, or any of its decade outputs. To speed up measurements at the end of the display hold time, the counter is preset to 99,999,9XX during the display hold. (X indicates that the least significant digits are not preset.) Within one hundred counter trigger periods the selected time base will overflow to start the error rate measurement.

BIT RATE/BLOCK RATE MEASUREMENTS

In the preceeding discussion, it was assumed that the MB-1A was placed in bit error rate mode. This means that bit error pulses (one for each erroneous data bit) are triggering the error counter. Error rate display will then be bit errors per period of time (time rate), bit errors per number of frames (frame rate), or cumulative bit errors (totalize).

Another form of error measurements is possible with MB-1A. These are block error measurements, where a single error pulse is generated for each data block containing one or more bits in error. The selection of block error rate will affect the error counter trigger input in all three measurement modes previously discussed. Further, it affects the clock signal driving the time base counter by dividing the input clock by the block size selected. Block sizes of 10 bits, 100 bits, or 1000 bits may be selected.

Block rate logic is located on the RESYNC CONTROL card. The small time base counter used by the synchronization threshold logic is shared with the block rate logic. This consists of a multiplexer which selects the appropriate decade of the sync time base counter as the clock signal to the main time base counter on the COUNTER card. (In bit error rate this multiplexer selects the input clock itself.) The selected decade drives the reset of a latch which is set by any bit error pulse generated by the bit error detector. This creates a single error pulse to the error counter, irregardless of how many bit errors have occurred during the block.

With block rate selected, the error rate display will be block errors per number of blocks (time rate), block errors per number of frames (frame rate), or cumulative block errors (totalize).

CLEAR FUNCTION

The clear function is generated on the INTERFACE and PRINTER card, where the pushbutton and front panel signal are logically or'ed. They drive the reset signal to the RESYNC CONTROL card, where the counters are cleared and placed into "in sync" status.

A remote input clear is logically or'ed with the front panel clear function to generate a reset signal to the COUNTER card, where the time base counter is preset and the first decade of the error counter is cleared. A display clear is generated on that card which clears the rest of the error counter and the display.

ERROR DISPLAY

BCD outputs of the first error counter decade drive a decoder/display IC. The second error counter decade is also a higher speed BCD counter IC driving a decoder/display IC. Remaining decades of the error counter are lower speed; therefore integral BCD counter/decoder/display IC's are used. The most significant stage of the error counter drives the overflow latch. All of this logic is located on the DISPLAY card, mounted behind the front panel.

PRINTER CONTROL

Logic on the INTERFACE and PRINTER card controls the printer I/O.

Internal print strobes are only generated during frame rate or time rate modes because the GATE TIME signal is used to trigger the print strobe. At the same time, the GATE TIME signal also triggers the display hold time out (located on the COUNTER card) which freezes the display for approximately 1.6 sec to allow visual read out of display value.

Either GATE TIME or the remote $\overline{\text{INTERROGATE}}$ signal will trigger a PRINT STROBE. RC timing components of a 74123 determine the width of PRINT STROBE. A jumper on one input of the exclusive-or driver gate determines the PRINT STROBE polarity. During the PRINT STROBE the display is frozen.

A Busy input from the printer will keep the display frozen while the printer cycles. A jumper on one input of the exclusive-or receiver gate determines BUSY polarity. At the trailing edge of BUSY, a hold off timer is triggered to keep the display frozen until the printer is ready to accept a change in data. RC timing components of 74123 determine the length of the hold off time.

For interfacing to other controllers, such as a computer, a ENABLE (DATA LOGGING) input is provided which disables the internal display strobe, thus freezing the display for any length of time desired.

In order that these hold off controls should not interfere with MB-1A operation when a printer is not connected, an input (PRINTER OFF) is provided to sense whether or not a printer is connected. When there is no printer the PRINT STROBE and BUSY signals are disabled.

BACK-TO-BACK TESTING OF THE MN-1 AND MB-1A

MN-1 SET UP

1. Set mode selection to FEEDBACK.
2. Set CODE LENGTH SELECTION to 6.
3. Connect a clock source to CLOCK IN at standard TMI levels.
4. Insure that the CLOCK TRIG'D indicator is lit. If not, re-check levels.
5. If clock is triggered properly, the RUN indicator will be lit.
6. Connect the SYNC OUT (terminated in 50 ohms) to external sync input of oscilloscope.
7. Monitor CLOCK OUT and insure that the signal is a good pulsed waveform. If not, readjust the input level.
8. Monitor DATA OUT terminated into 50 ohms and vary input clock frequency from 75 MHz down to less than 1 Hz.
9. Change CODE LENGTH SELECTION and repeat #8; remember that the longer the sequence, the longer the time between sync pulses; i.e., at 1 MHz and 2^{20}-1 selected, it takes better than 1 second to sequence through one frame.

MB-1A SET UP

10. Adjust two coaxial cables connected from MN-1 CLOCK OUT and DATA OUT such that the DATA OUT cable should be about 40 inches (5 ns) longer than the clock cable. This will assure that the power phase relationship is maintained within the MB-1A for all frequencies from 75 MHz to 1 Hz with the phase control fully counter clockwise.
11. Connect the MN-1 CLOCK OUT into the MB-1A CLK IN and insure that the CLK TRG'D LED and RUN indicator are lit.
12. Set SYNCHRONIZATION mode to MANUAL. Set REF DATA to PN.
13. Select ERROR RATE BASE to BIT RATE "1"; select FRAME (SYNC) and TIME BASE SELECTION to 10^N where N = 0. Since the data input is open circuited, the MB-1A considers the logical "1's" of the selected sequence to be in error approximately 50% of the time.

MB-1A SELF TEST

14. The display counter should now count the amount of "1's" in the selected sequence. For:

2^N-1 where N = 6 ERROR COUNTER reads 32.
= 9 ERROR COUNTER reads 256.
= 11 ERROR COUNTER reads 1,024.
= 15 ERROR COUNTER reads 1 6,384.
= 17 ERROR COUNTER reads 1 5,536.
= 20 ERROR COUNTER reads 1 4,288.

The counter will count all errors in the frame and when the counter exceeds 9999, it overflows but continues to count and retain the lower four LSB; i.e., for N = 15 or 32,767 bit sequence, there are 16384 ones; the numbers 6384 are displayed and 1 is the overflow.

15. Now change TIME BASE SELECTION to 10^N where N = 1. The count will be integrated over 10 frames; i.e., for CODE LENGTH SELECTION 2^N-1 where N = 6, counter reads 32 with TIME BASE SELECTION = 10^0 and for TIME BASE SELECTION = 10^1 counter reads 320.

16. When changing to TIME RATE, depress CLEAR and set TIME BASE SELECTION for 10^1 through 10^{10}. 10^N for N = 0 is invalid.

17. In changing TIME BASE SELECTION, it is a good policy to clear the counter by depressing the CLEAR pushbutton.

18. With no data input, TIME RATE and TIME BASE SELECTION = 10^3 selected, the counter will read around 500, or out of any 1,000 bits approximately 50% will be in error.

19. Check CLOCK OUT and ERROR OUT to insure proper signals.

20. Adjust frequency to 10 MHz. Now monitor CLOCK OUT and clock source. Adjust PHASE control and insure greater than 30.0 ns of delay. Even though the clock delay adjustment will operate over all frequencies, the overall duty cycle may not exceed -5ns i.e., an operating frequency of 40 MHz (25 ns period) allows a maximum delay of only 7.5 ns. Return PHASE to fully counter clockwise.

21. Select ERROR RATE BASE, BLOCK RATE, 10; the counter will examine block of 10 bits and if 1 or more bits are in error, the counter will count 1 error. The TIME BASE SELECTION = 10^3. The display will show 1,000 or all block in error except when the longer sequences are chosen, then it is possible that some blocks will be correct and the counter will count around 993. As the block is extended to 100 and 1,000, there are no consecutive blocks or 100 or 1,000 zero, therefore, for all sequences, all blocks will be in error.

MN-1/MB-1A TEST

22. Connect MN-1 DATA OUT to MB-1A DATA IN (Check step #10) and insure that CODE LENGTH SELECTION for MN and MB are the same.

23. The DATA TRG'D and PHASED LEDS should light.

24. Select LOW error THRESHOLD. Select BIT RATE, FRAME (SYNC) and TIME BASE SELECTION N = 0. Depress the MANUAL sync button. The system should synchronize; SYNC light should go on and the BURST ERROR light go off. The ERROR COUNT will read all zeros.

25. Select a different sequence length on both MN and MB and synchronize by depressing MANUAL. Remember they must be the same length.

26. With the system synchronized, depress the TEST pushbutton on the MN-1 and notice that the system will fall out of sync. SYNC light out and BURST ERROR ON. Resync manually.

27. Change to AUTO SYNCHRONIZATION and depress TEST: note system automatically synchronizes. Repeat for various sequence length and frequencies.

28. Select a lower clock frequency of approximately 10 kHz; select HIGH THRESHOLD: TOTALIZE: depress and hold TEST and watch counter count up to 20,000 errors and then signify out of sync. Notice that the system will automatically search and attempt synchronization until complete and the SYNC LED will light.

29. Select EXTERNAL COMMAND SYNCHRONIZATION. Depress TEST once and with an external source at standard TMI levels, pulse the external command. Resynchronization will occur.

30. In the TIME RATE or FRAME rate mode, apply a TMI signal to the gate input and the system in error. Notice how the counter will be inhibited.

31. Monitor TIME BASE OUT for selected time base and insure operating properly.

LIST OF ILLUSTRATIONS

MB-1 Block Diagram. TCN-53178

Module Power Supply TAJ-53385

MB-1A Pseudorandom Number Generator Schematic TDJ-53617

MB-1A Error Accumulator and Resync Control Schematic. . . TDJ-53616

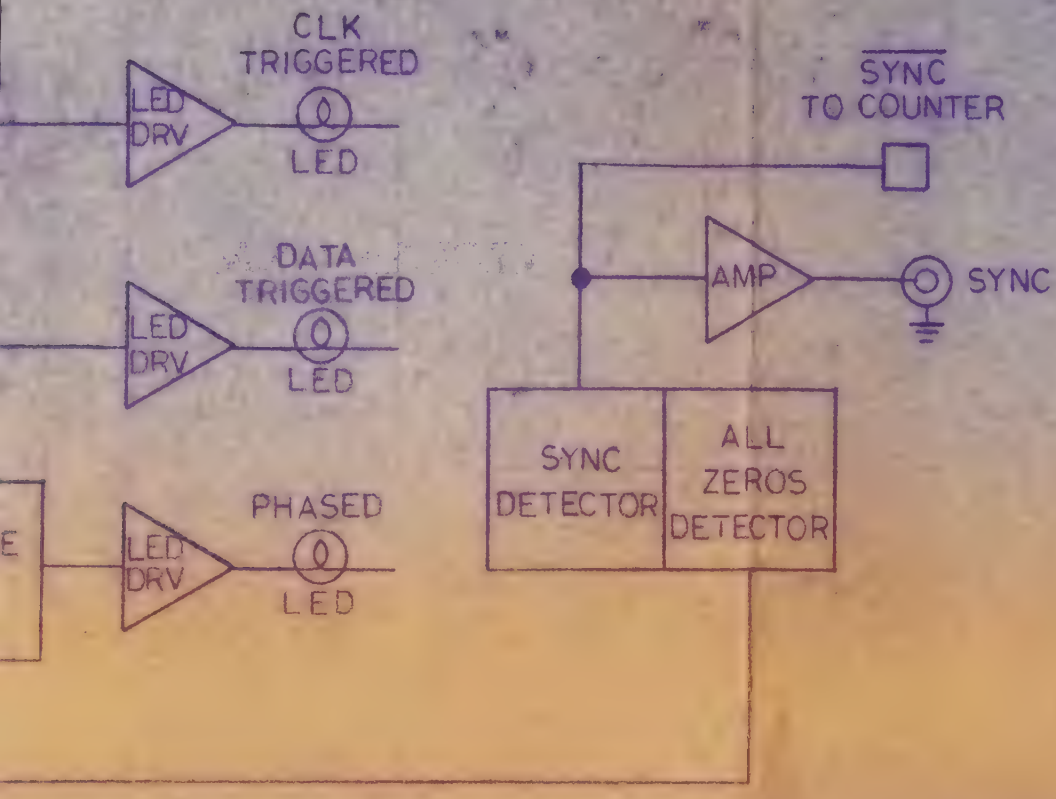
MB-1A Interface and Printer Option. TDJ-53553

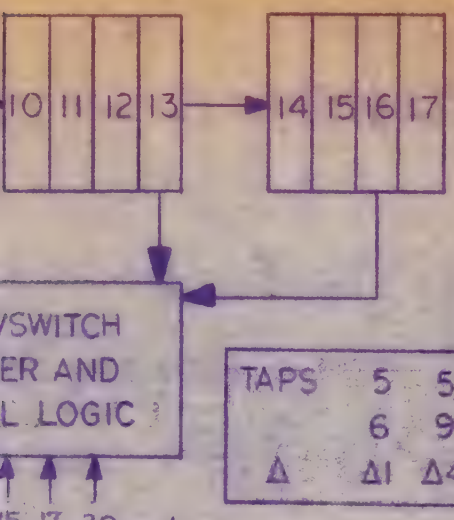
MB-1A Counter Schematic TDJ-53893

MB-1 Counter Display Schematic. TCJ-53014

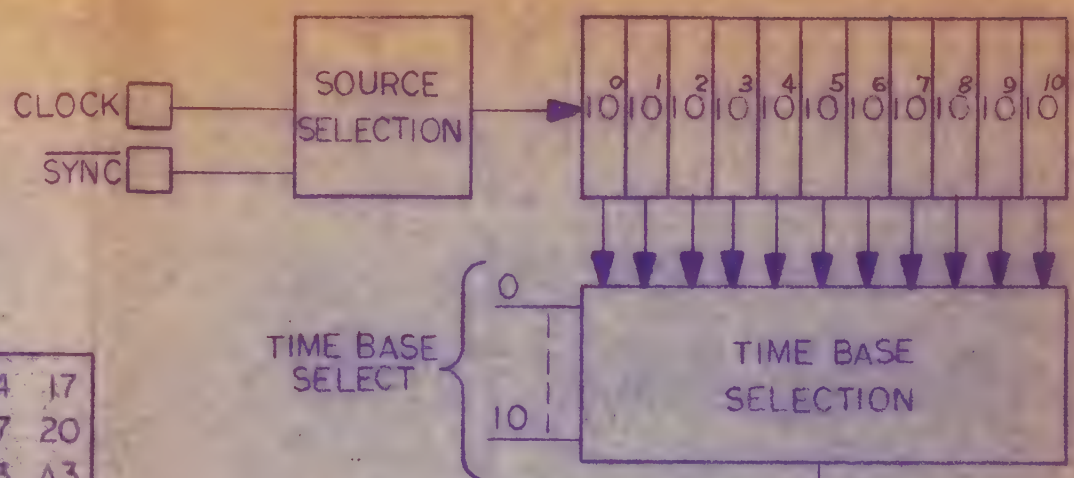
30 nSEC DELAY CIRCUIT
CLOCK
PRE AMP
51Ω
MONO STABLE
CLOCK DISTRIBUTION
CL-1
CL-2
CL-3
CL-4
CL-5
CL-6
CL-7
CL-8
CL-9
TOGGLE FF
TOGGLE FF
CLK ERROR ACCUMULATOR
DATA
PRE AMP
DATA INPUT FF
CL-1
LED DRV
RUN
LED
PHASE DET FF R
TOGG FF
RE SYNC CMD
MODE CONTROL FF
CL-2
RE SYNC
FEED BACK
FEEDBACK CONTROL LOGIC
S
1
2 3 4 5
6 7 8 9
Δ5
CONTROL GATE
TAP SEL
TAP SEL
TAP SEL
TAP SEL
DIOD DECO CONTR
6 9 11
SWITCH
ERROR
Q
CL
Δ1 Δ2 Δ3 Δ4
DATA
ERROR
÷2 ERROR
10' ERROR COUNTER
10³ ERROR COUNTER
20X10³
20
SEL LO
ERROR TO COUNTER
BLOCK ERROR FF
MONOSTABLE
AMP
ERROR
R
10³
10⁵
ERROR COUNTER RESET
SEL HI
SEL LO
CLOCK
÷10
÷100 ÷10³ ÷10⁴ ÷10⁵
AUTO
CMD EXT
CMD
51
RE SYN SELECTO
MANUAL
BIT/BLOCK RATE SELECTOR
MONOSTABLE
AMP
CLOCK
CLOCK COUNTER
BIT 10 100 1000
SELECT RATE

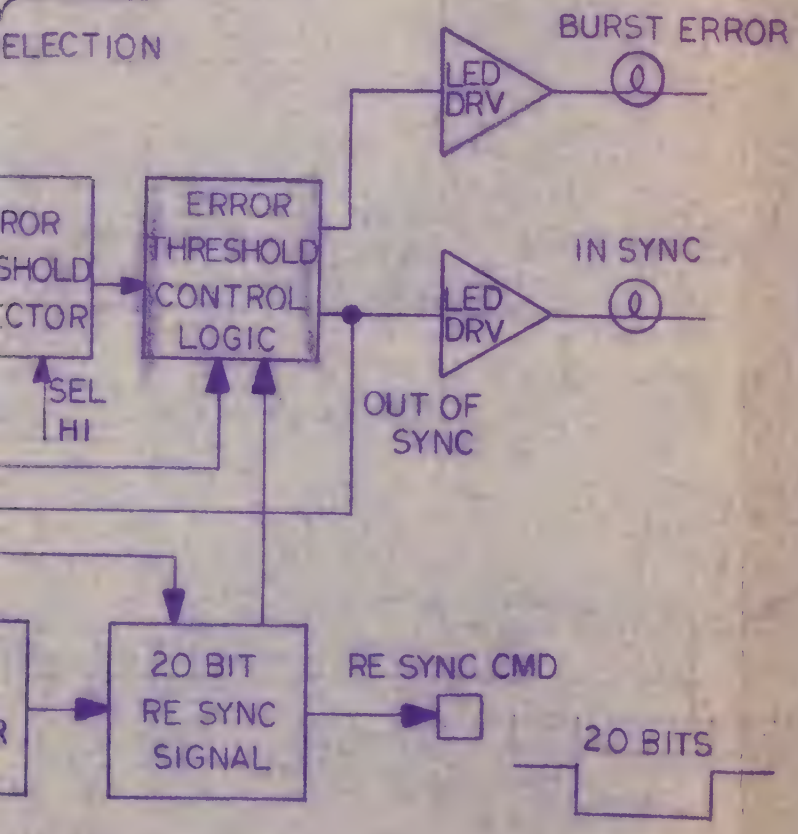
CHARLES BRUNING CO. – FIVE HUNDRED

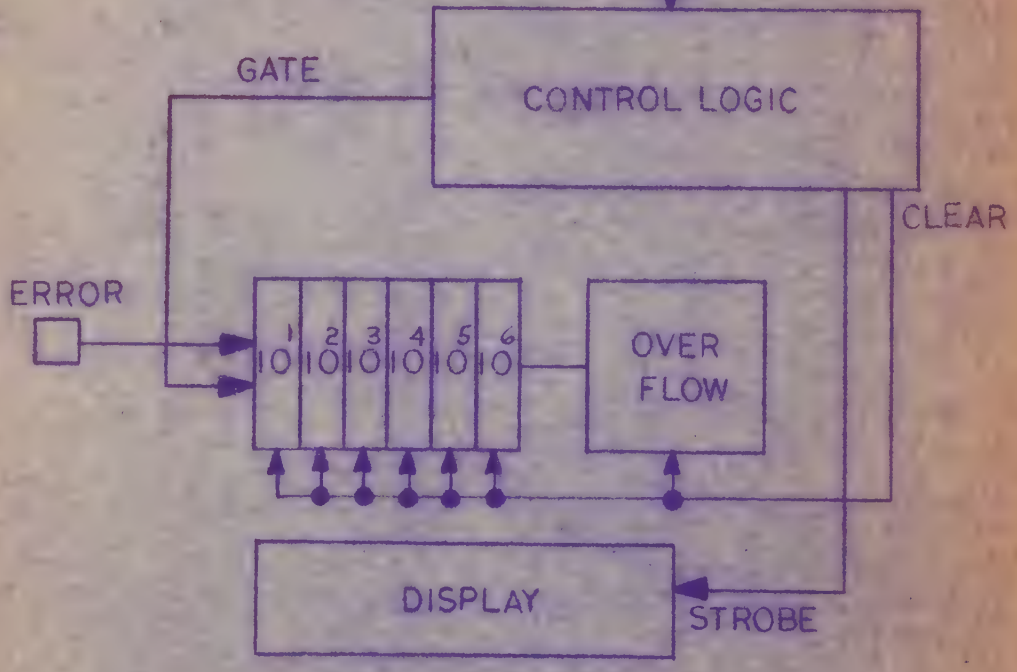




TAPS	5	5	9	14	14	17
	6	9	11	15	17	20
Δ	Δ1	Δ4	Δ2	Δ1	Δ3	Δ3





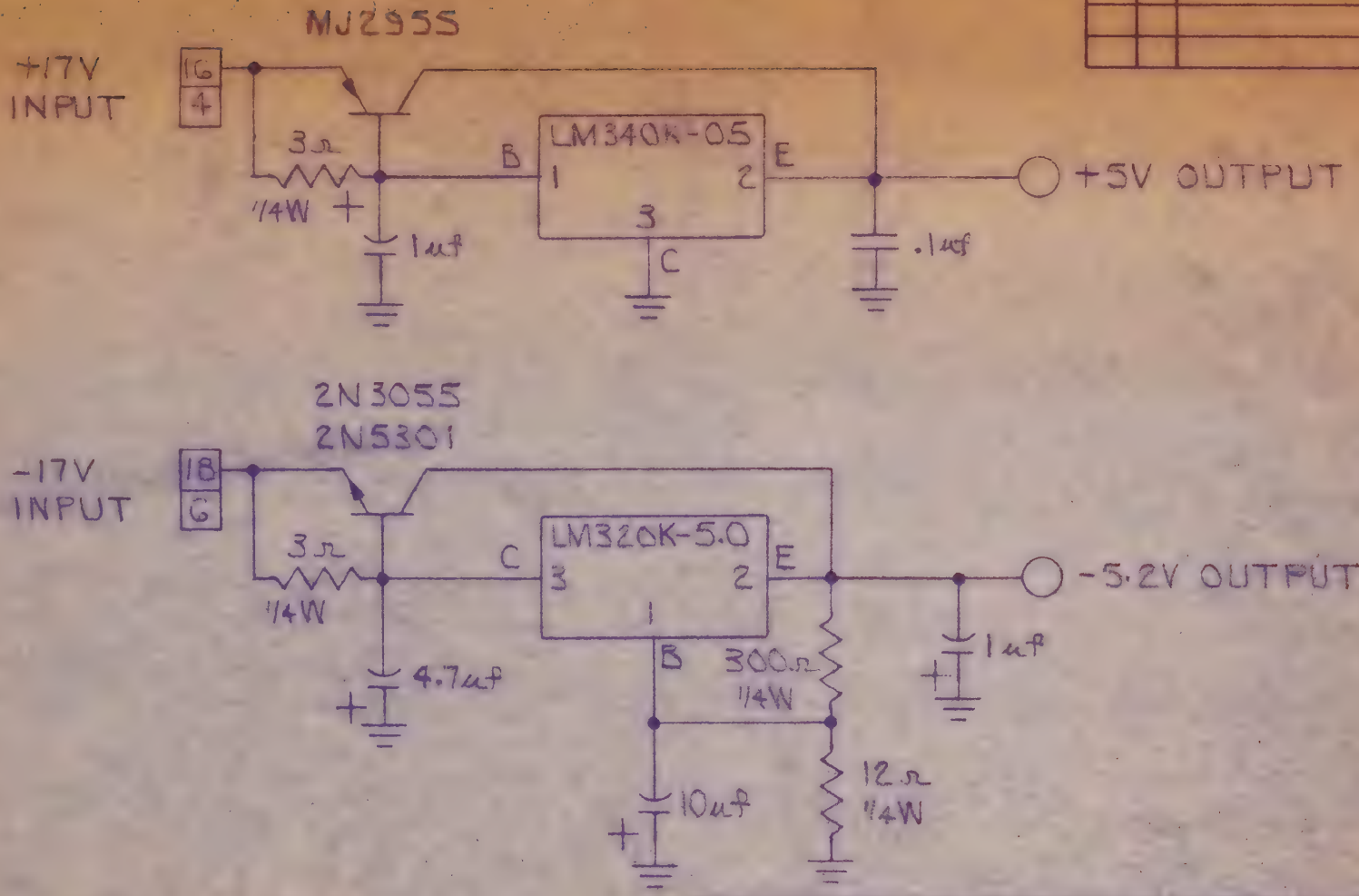


TMI

TAU-TRON, INC.

SCALE TM	REVISIONS	BY	DATE
DATE 11-10-73			
DR'N. AHH CK'D.			
AP'VD.			
TITLE BLOCK DIAGRAM MB-1		NO. TCN-53178	

		REVISION RECORD	BY	CK



TOLERANCES (EXCEPT AS NOTED)	TAU-TRON INC.	
DECIMAL ±	TMI SERIES	SCALE — DRAWN BY Jon Bentalow APPROVED BY
FRACTIONAL ±	TITLE SCHEMATIC MODULE POWER SUPPLY (±5V Boost)	
ANGULAR ±	DATE 11 5 74	DRAWING NUMBER TAJ-53385

BRUNING 40-21

NOTES:

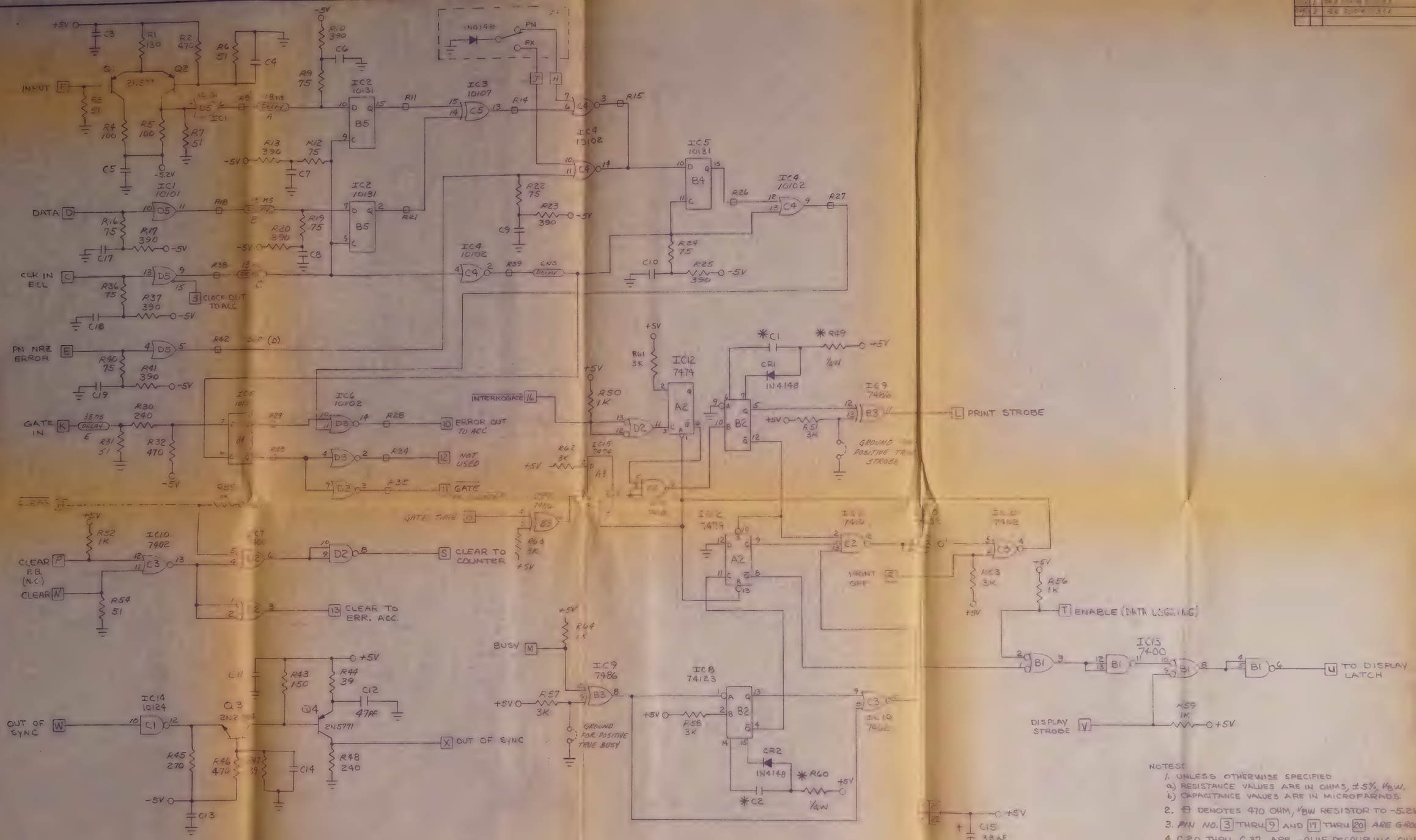
1. UNLESS OTHERWISE SPECIFIED:
   RESISTORS, VALUE IN OHMS, 1/8 W, 5%
   CAPACITORS; ARE .01 μF
   DIODES; ARE 1N4148
2. ⊟ = 470 Ω TO -5.2V (PULL DOWN)
   74 PLACES
3. ⊡ = EDGE CONNECTOR PIN NO. OF LETTER
4. ⊗ = 16 PIN CABLE CONNECTOR FROM LOCAL/REMOTE LOGIC BOARD (E1).

SELECTION	TAPS	Δ
1	5 & 6	1
2	5 & 9	4
3	9 & 11	2
4	14 & 15	1
5	14 & 17	3
6	17 & 20	3

REF DRAWINGS
MB1A LOADING DIAGRAM TDK53187
MB3 LOADING DIAGRAM TDK53697

TOLERANCES (EXCEPT AS NOTED)	TAU TRON INC.
DECIMAL	TMI SERIES
FRACTIONAL	TITLE MB-1A/MB-3 MASTER CLOCK GENERATOR SCHEMATIC
ANGULAR	DATE 2-6-74 DRAWING NUMBER TDK-53617 REV 2
SCALE	DRAWN BY
APPROVED BY	

THRESHOLD (FRONT PANEL) S-502
HI
LOW
ERROR INPUT
E201
IC201 10102
B5
R201 68
R202 390
C201
-5.2V
B4 10131 IC202
IC203 10125
C5
VBB
E5 74196 IC204
E4 7490 IC205
E3 7490 IC206
IC209 74H01
D1
FROM INTERFACE BOARD
RESET
R275 1K
+5V
E203
ERROR OUT ECL
TO COUNTER
R206 22
+5VO
C204 47pf
R208 150
IC201 10102
B5
Q201 2N2784
Q202 2N5771
E202
ERROR OUT
TO FRONT PANEL
R204 270
R205 39
C203
R210 240
CR201 1N4148
B4 10131 IC202
R203 100
C202 47pf
R211 1K
R212 1K
R213 1K
R214 1K
R215 1K
IC208 74H01
E1
F1 74LS74 IC210
R216 1K
R217 1K
IC209 74H01
F5 SN7407 7401
C205 1000 pf
RESYNC TTL
F3 74123 IC211
R219 30K
C207 10 pf
R218 20K
10 VOLPT
F4 7474A IC212
F TO INTERFACE BOARD FOR AMPLIFICATION
R220 150
BURST ERROR IND
LED
R221 150
IN SYNC
LED
D2 7400
IC213 7400
NOTES
CLOCK INPUT
E205
IC223 10102
B2
R222 68
C208
R223 390
-5.2V
B3 10131 IC213
C4 10131 IC214
IC203 10125
C5
VBB
D5 7490 IC215
D4 7490 IC216
D3 7490 IC217
R224 1K
R225 1K
AUTO M
EXT P
MANUAL K
+5VO MANUAL SYNC FRONT PANEL S503
R226 51
R227 1K
R228 470
R229 470
IC219 74H52
F2
R230 1K
F1 74LS74 IC210
BLOCK RATE (FRONT PANEL)
S505
100
1000
R231 1.2K
R232 2K
B1 10102 IC220
C3 10131 IC221
R235 470
R234 470
R235 470
R236 470
R237 1K
R238 1.2K
IC222 74H52
C2
R240 1.2K
R241 2K
IC223 10102
R239 2K
IC220 10102
E207
RESYNC
TO P.R. NUMBER GEN.
F5 SN7407 7401
RESYNC TTL
IC203 10125
C5
VBBO
IC220 10102
B1
R242 100
C209 100pf
E206
CLOCK OUT ECL
TO COUNTER
C210
R246 150
Q203 2N2748
Q204 2N5771
R248
C212 47pf
R243 270
R244 470
R245 39
C211
R249 240
E204
CLOCK OUT
TO FRONT PANEL
+5V
33µf 10V
-5.2V
(MAN)
(AUTO)
(EXT)
K
TO MANUAL ENABLE F2-4
M
TO AUTO ENABLE F2-12
P
TO EXT ENABLE F2-10
SYNCHRONIZATION (FRONT PANEL) S-504
ALL RESISTANCE VALUES ARE SPECIFIED.
ALL RESISTANCE VALUES ARE IN OHMS, ¼W ± 5%
ALL CAPACITANCE VALUES ARE IN MICROFARADS
R___ IS A 470Ω RESISTOR TO -5.2V.
( ) DENOTES EDGE CONNECTOR PIN # OR LETTER
UNMARKED CAPACITORS ARE .01µf CHIP.
REFERENCE DWGS
LOADING - TDK-53845
DRILL -
TT1194
EFFECTIVE S/N 8330271
TAU-TRON, INC.
TMI-SERIES
TDK-53616



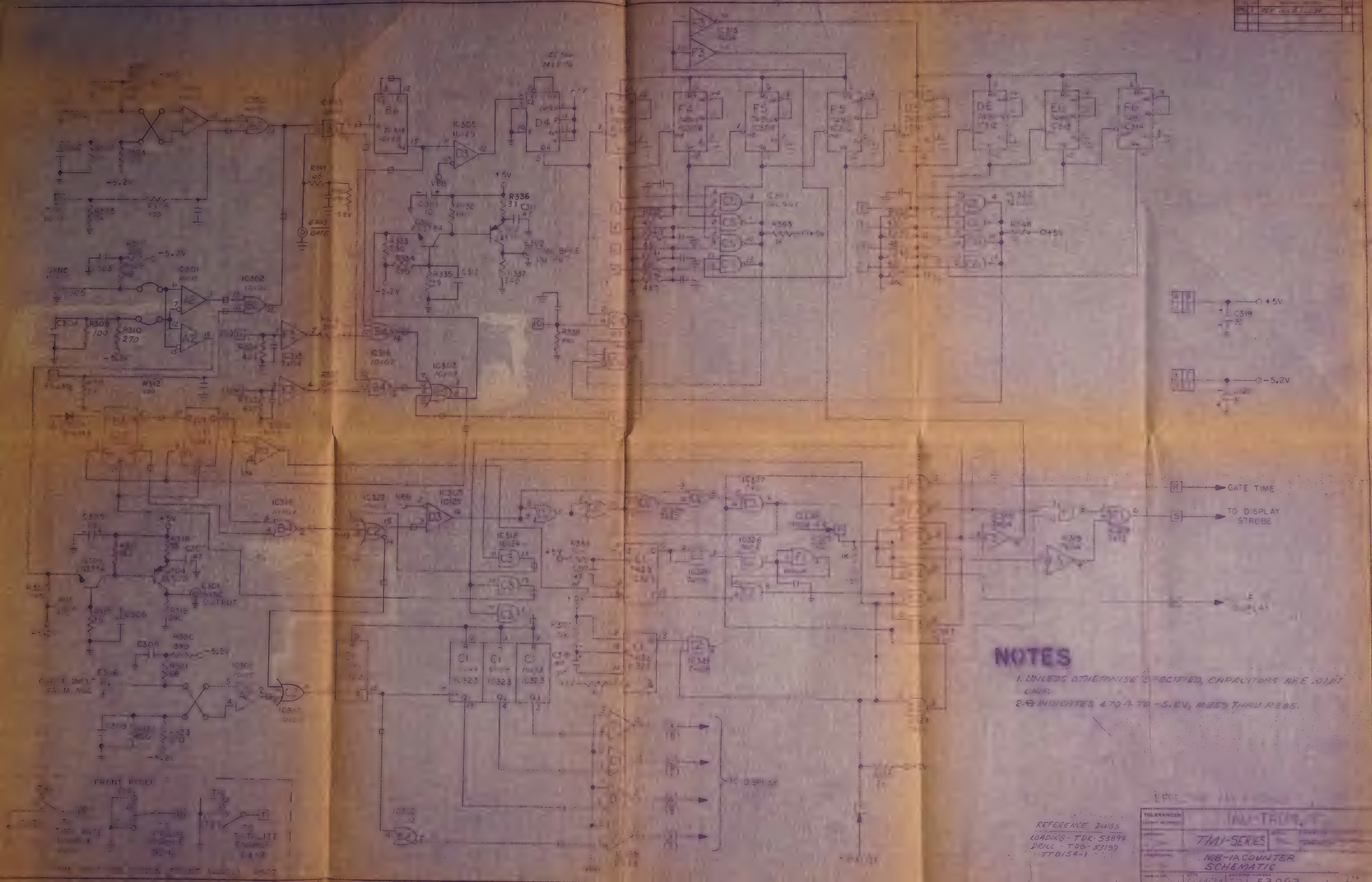
NOTES:

1. UNLESS OTHERWISE SPECIFIED
   a) RESISTANCE VALUES ARE IN OHMS, ±5%, ½W.
   b) CAPACITANCE VALUES ARE IN MICROFARADS.
2. ⊕ DENOTES 470 OHM, ½W RESISTOR TO -5.2V
3. PIN NO. 3 THRU 9 AND 17 THRU 20 ARE GROUND.
4. C20 THRU C37 ARE .01 UF DECOUPLING CHIP CAPS
5. ✱ TO BE DETERMINED IN TEST.
6. UNMARKED CAPACITORS ARE .01 UF

LAST DESIGN NUMBERS USED			
R64	C37	Q4	
IC15	CR3		

REF DWG'S
DRILLING - TBG-53548
LOADING - TDK-53549

TOLERANCES (EXCEPT AS NOTED)	TAU-TRON, INC.		
DECIMAL	TM1/MB-1A	SCALE ¾	DRAWN BY A. [illegible]
FRACTIONAL	TITLE INTERFACE & PRINTER OPT.		APPROVED BY
ANGULAR	DATE 3-14-75	DRAWING NUMBER TDJ-53553	



IC305
10125
D3
VBB
D4
+5V
R336
33
C311
47
E302
TIME BASE OUTPUT
R349
68
E303
GATE
IC301
10115
A2
IC302
10102
R309
100
R310
270
-5.2V
IC315
7404
F3
IC316
10102
B4
IC303
10109
R333
240
R334
270
R335
39
R337
240
R338
430
F4
IC308
F5
R343
1K
D6
E6
F6
C314
R348
C319
IC319
10102
IC322
IC318
10124
C3
C2
C1
IC323
R318
33
E301
SYNC OUTPUT
R319
240
C306
C308
R320
390
R321
68
R323
270
IC304
10115
FRONT PANEL
TO DISPLAY
IC327
IC326
IC324
GATE TIME
TO DISPLAY STROBE

NOTES

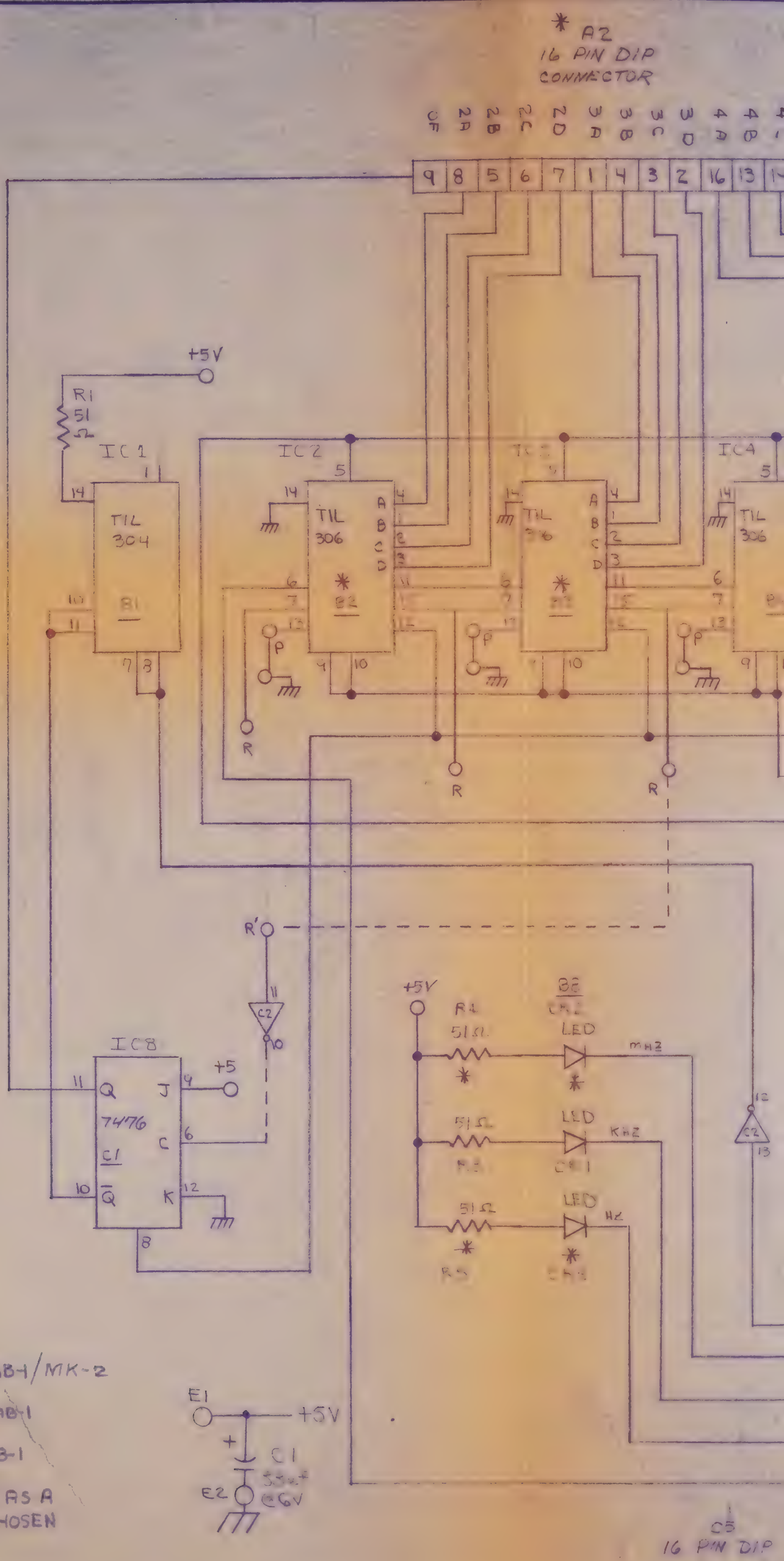
1. UNLESS OTHERWISE SPECIFIED, CAPACITORS ARE .01µF CHIP.
2. ⊟ INDICATES 470 Ω TO -5.2V, R359 THRU R385.

REFERENCE DWGS
LOADING - TDK-53894
DRILL - TDG-53197
TT0154-1

TOLERANCES

TMI-SERIES

MIB-1A COUNTER SCHEMATIC



NOTES

1 - * = OPTION NOT USED IN MB-1/MK-2

2 - TIE ALL "P" TO GND FOR MB-1

3 - TIE "P" TO KHZ LED FOR MB-1

4 - TIE R' TO COUNTER DISPLAY AS A FUNCTION OF OPTION CHOSEN

DATE	SYM	REVISION RECORD	DR	CK
8/16	1	DCN #00187		

* A1
16 PIN DIP
CONNECTOR

5A 5B 5C 5D 6A 6B 6C 6D 7A 7B 7C 7D

4 D | 15 | E506 | 5 | 8 | 7 | 6 | 1 | 4 | 3 | 2 | 16 | 13 | 14 | 15 | E507

IC5 TIL 306 (E8)

IC6 TIL 308 (A6)

IC7 TIL 308 (B7)

IC9 74H01 (C2)

IC10 C3 74196

IC11 74H00 (C4)

R2 2K +5V

R6 2K +5V

P P' H H N N

D C B A

A	1	2	3	8	9	10	11	15	12	13	16	14	ESAS
BLANK IN	HZ	KHZ	MHZ	GATE TIME	STROBE	DECIMAL POINT/GATE TIMING	CLEAR	ENABLE	D	C	B	A	

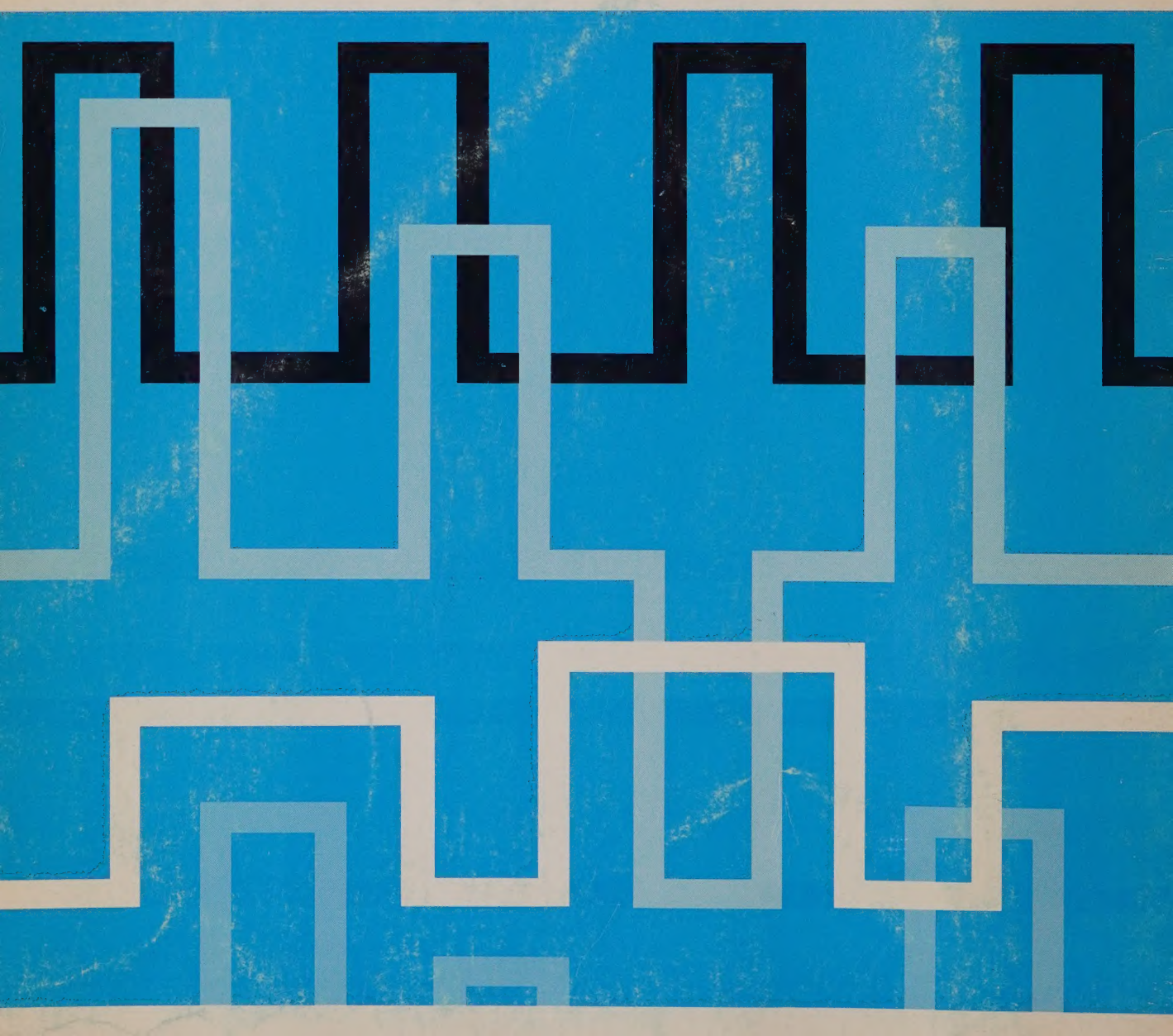
TOLERANCES (EXCEPT AS NOTED)	TAU-TRON INC.		
DECIMAL ±	TMI	SCALE:	DRAWN BY:
FRACTIONAL ±	TITLE: COUNTER DISPLAY BD. SCHEMATIC		APPROVED BY
ANGULAR ±	DATE: 5-29-73	DRAWING NUMBER: TCJ-53014	REV: 1

tau-tron inc
11 Esquire Road, North Billerica, Mass. 01862
Tel: (617) 667-3874 TWX: 710-347-1570

WARRANTY

All Tau-Tron products are warranted against any defects in material and workmanship. This warranty applies for one year from the date of delivery for all Tau-Tron manufactured products. The warranty period for OEM products sold by Tau-Tron will depend on the original OEM warranty (consult factory for specific products). We will repair or replace products which, upon our examination, prove to be defective during the warranty period. NO OTHER WARRANTY, EXPRESS OR IMPLIED, INCLUDING FITNESS FOR PURPOSE, MERCHANTIBILITY, OR OTHERWISE, IS GIVEN.

For any assistance, contact the factory and be prepared to provide instrument model and serial numbers and all details regarding the malfunction.

TAU-TRON, INC.
11 Esquire Road
North Billerica, Massachusetts 01862 USA
Telephone: 617-667-3874
TWX: 710-347-1570

tau-tron
inc
11 Esquire Road, North Billerica, Mass. 01862
Tel: (617) 667-3874